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L1: (9) "704"/\$.ccls. and dual adj access

L2: (0) "704"/231.ccls. and dual adj access

L3: (775) "704"/231.ccls.

L4: (71) "704"/231.ccls. and front adj end

L5: (0) "704"/231.ccls. and daram

L6: (2) "704"/\$.ccls. and daram

L7: (1) "704"/\$.ccls. and staiger.in.

L8: (38) "704"/231.ccls. and front adj end and @ad<"20010314"

L9: (174) "711"/\$.ccls. and speech adj recognition

L10: (73) 9 and @ad<"20010314"

L11: (8) "711"/\$.ccls. and speech adj recognition and (dual adj access or daram)

USPUB:USPAT

Default operator: OR

*711"/\$.ccls. and speech adj recognition and (dual adj access or daram)

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	U	K1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cl	Inventor	S	C	P	③	Imt
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20030200410 A	20031023	48	Memory management in embedded systems with dynamic	711/170	711/165		Russo, David A. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6968438 B1	20051122	44	Application programming interface with inverted memory or	711/170	717/100		Russo, David A. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US
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4	<input type="checkbox"/>	<input type="checkbox"/>	US 6691298 B1	20040210	57	Memory management in embedded svstam with dynamic	717/100	711/170; 717/100		Russo, David A. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6546477 B1	20030408	44	Memory management in embedded svstam with desion ti.	711/170	717/100		Russo, David A. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6363470 B1	20020326	22	Circular buffer management	711/220	710/56; 711/110		Laurenti, Gilbert et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5983328 A	19991109	32	Data processing device with time-multiplexed memory bus	711/157	711/150		Potts, James F. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5907864 A	19990525	31	Data processing device with time-multiplexed memory bus	711/169			Potts, James F. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US

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NUM

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
19 September 2002 (19.09.2002)

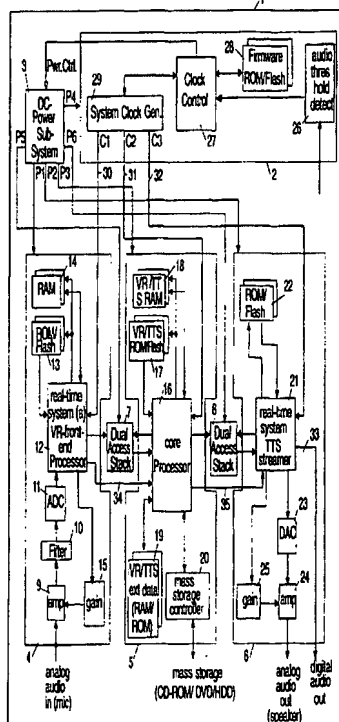
PCT

(10) International Publication Number
WO 02/073600 A1

- (51) International Patent Classification: G10L 15/28 (72) Inventor, and
(75) Inventor/Applicant (for US only): STAIGER, Dieter
(21) International Application Number: PCT/EP02/01636 (DB/DE); Falkenstrasse 28, 71093 Weil im Schönbuch (DE).
(22) International Filing Date: 15 February 2002 (15.02.2002)
(25) Filing Language: English (74) Agent: KLEIN, Hans-Jörg; IBM Deutschland GmbH, Intellectual Property, Pascalstr. 100, 70548 Stuttgart (DE).
(26) Publication Language: English (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW.
(30) Priority Data: 01106231.2 14 March 2001 (14.03.2001) EP
(71) Applicant (for all designated States except US): INTERNATIONAL BUSINESS MACHINES CORPORATION (US/US); New Orchard Road, Armonk, NY 10504 (US).
(71) Applicant (for LU only): IBM DEUTSCHLAND GMBH (DE/DE); Pascalstrasse 100, 70549 Stuttgart (DE).
(84) Designated States (regional): ARIPO patents (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW). Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM).

[Continued on next page]

(54) Title: METHOD AND PROCESSOR SYSTEM FOR PROCESSING OF AN AUDIO SIGNAL.



(57) Abstract: In a processor system (1) for audio processing, such as voice recognition and text-to-speech, a dedicated front-end processor (12), a core processor (16) and a dedicated back-end processor (21) are provided which are coupled by dual access stack (7) and (8), respectively. When an analog audio signal is inputted core processor (16) is invoked only when a certain amount of data is present in the dual access stack (7). Likewise the back-end processor (21) is invoked only when a certain amount of data is present in the dual access stack (8). This way the overall processing power required by the processing task is minimised as well as the power consumption of the processor system (1).

WO 02/073600 A1

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L11: Entry 8 of 19

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Sep 19, 2002

PUB-NO: WO002073600A1

DOCUMENT-IDENTIFIER: WO 2073600 A1

TITLE: METHOD AND PROCESSOR SYSTEM FOR PROCESSING OF AN AUDIO SIGNAL

PUBN-DATE: September 19, 2002

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APPL-NO: EP00201636

APPL-DATE: February 15, 2002

PRIORITY-DATA: EP01106231A (March 14, 2001)

INT-CL (IPC): G10L 15/28

EUR-CL (EPC): G10L015/28

ABSTRACT:

CHG DATE=20021101 STATUS=N>In a processor system (1) for audio processing, such as voice recognition and text-to-speech, a dedicated front-end processor (12), a core processor (16) and a dedicated back-end processor (21) are provided which are coupled by dual access stack (7) and (8), respectively. When an analog audio signal is inputted core processor (16) is invoked only when a certain amount of data is present in the dual access stack (7). Likewise the back-end processor (21) is invoked only when a certain amount of data is present in the dual access stack (8). This way the overall processing power required by the processing task is minimised as well as the power consumption of the processor system (1).

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